Texas Instruments

TLC4541 EVM

User's Guide

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of ±12 V and the output voltage range of ±12 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Chapter 1

Introduction

This chapter contains an overview of the features and functions of the EVM.

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This user's guide has been written to help you get the most from your evaluation module (EVM). The TLC4541 EVM is a member of the multipurpose (MP) family of serial EVMs. It provides a platform to demonstrate the performance and functionality of the TLC4541 ADC and the TLV5636 DAC.

TI's websites are regularly updated. They present the latest software additions, development information, troubleshooting help, general background, as well as all applicable data sheets.

For specific questions related to this EVM or device send an email to the Analog Applications Team at *dataconvapps@list.ti.com* and reference the orderable tool description – *TLC4541 EVM*.

This user's guide is divided into the following chapters:

- Chapter 1 offers an overview of the EVM and introduces the general features and functions of the system.
- Chapter 2 describes the operation of the EVM from a user's view. It details options that can be modified, connectors used, and pinout details.
- Appendix A details the bill of materials (BOM) and the schematic, along with explanations of certain EVM features.

1.1 EVM Modes

This EVM has been designed, tested, and shipped in a condition that enables the user to begin evaluation with minimal effort.

There are basically two operating modes for the EVM. These modes are mutually exclusive. They are:

- **Stand-Alone Mode (SAM)**

  Stand-alone mode enables the user to check the system without the support of a signal generator, pattern generator, or DSP. In this mode, the digital output from the ADC is fed into the companion DAC and reconstructed.

  User mode is deselected if SAM is selected. The DSP will be unable to communicate with either the ADC or the DAC.

- **User Mode**

  The EVM typically operates via a DSP or a microprocessor. In this mode the user is responsible for generating all the control signals**.** If user mode is selected, SAM is deselected**.**

1.1.1 Stand-Alone Mode

A unique feature of this EVM is the facility it offers the user to closely couple the ADC and DAC with a minimum of user intervention. This feature allows the serial bit stream from the digitized analog output to be fed directly to the DAC. Therefore, the signal that is fed into the ADC can be reconstructed via the DAC. No DSP need be present.

SAM is selected by:

- ❏ Switching SW1-1 to the on position, LED is on.

1.1.2 User Mode

The user can connect the ADC to a DSP or to a microprocessor in two ways:

- ❏ Via IDC ribbon cable
- ❏ Via daughterboard connectors J16 and J17

User mode is selected by:

- ❏ Switching SW1-1 to the off position, LED is off.

For example, TI's range of DSP starter kits (DSK modules) provides a simple low-cost solution, offering a range of DSK modules for most needs. The EVM also supports the TMS320C6000 daughtercard specification (SPRA711), in addition to providing support for the Motorola specification for data transfer (SPI).

1.2 Analog Input Conditioning

There are a number of methods to connect analog input signals to the EVM. Chapter 2 discusses these alternatives.

1.3 Analog Output Conditioning

There are a number of methods to connect analog output signals to the EVM. Chapter 2 discusses these alternatives.

1.4 Prototype Area

An area of the PWB has been set aside if none of the signal conditioning options provided are suitable.

The prototype area has the following features:

- ❏ A matrix of plated-through holes (PTH)
- ❏ SMT pads in a standard 14-pin JEDEC footprint
- ❏ Convenient points to pick up all power options

Chapter 2

Getting Started

This chapter describes how the user can modify the various options of this EVM.

Topic **Page**

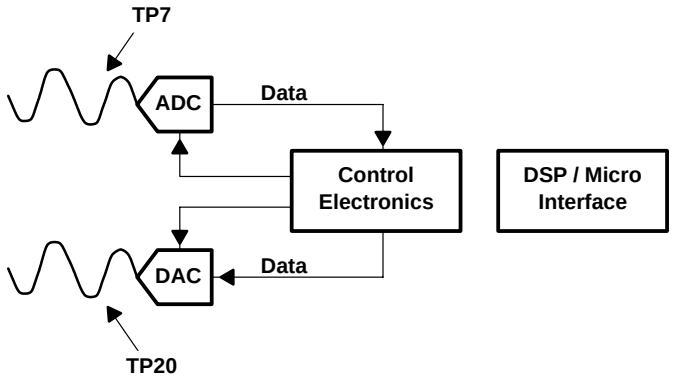
It is very important that users feel comfortable with the EVM from the beginning. To achieve this, each unit is manufactured and shipped in a predetermined condition. This allows the user to begin evaluation of the system immediately and to have confidence that the EVM is working.

To confirm that the EVM is working properly, follow the steps below:

1) Apply power to the system. The green LED will illuminate.
2) Ensure stand-alone mode (SAM) LED is on.
3) Check TP7 via oscilloscope. This will be a sine wave.
4) Press the reset button SW3.
5) Press the start button SW2.
6) Check TP20 with an oscilloscope. If the system is working properly, the signal at TP20 will also be a sine wave.

The system works as illustrated below. Any analog input supplied to the ADC will be digitized and reconstructed by the DAC.

Figure 2–1. SAM Configuration



The user may probe the data and control signals to observe the signals that allow stand-alone mode to function.

2.1 Shipping (Default Configuration)

The EVM is tested and shipped with jumpers and switches in a predetermined arrangement. This arrangement enables users to verify at once that the EVM is working. The tables below list switch and jumper settings that the EVM should be set to upon receipt.

Table 2–1. Default Switch Settings

Switch Settings		
	Default Configuration	**Description**
SW1-1	On	Stand-alone mode is selected, LED is on
SW1-2	Off	Reserved
SW1-3	Off	Reserved
SW1-4	Off	Reserved

Table 2–2. Default Jumper Settings

Jumper Settings			
	Default Configuration		**Description**
	Pins 1–2	Pins 2–3	
W1	Inserted	Not inserted	Input for channel 0 is via BNC connector J1.
W2	Not inserted	Inserted	Sine wave test signal is selected for channel 0.
W3	Not inserted	Inserted	Sine wave test signal is output for channel 0.
W4	Not inserted	Inserted	Onboard conditioned input for channel 0 is selected.
W5	Not populated		Not populated
W6	Not populated		Not populated
W7	Not populated		Not populated
W8	Not populated		Not populated
W9	Not inserted		Disables onboard sine and triangle wave generator
W10	Inserted	Not inserted	SCLK routed to ADC
W11	Not inserted	Inserted	Signal conditioning output selected for channel 0
W12	Inserted	Not inserted	FS routed to ADC
W13	Not Inserted		5-V analog
W14	Inserted		EVM reference or DAC's on-chip reference selected.
W15	Not populated		Not populated
W16	Inserted	Not inserted	Selects internal or external reference
W17	Inserted	Not inserted	Determines EVM reference voltage
W18	Not inserted	Inserted	FS routed to DAC
W19	Inserted	Not inserted	Selects source of signal conditioning output from DAC
W20	Not inserted		These jumpers determine various options for supplying system clock. This has been designed to be as flexible as possible to accommodate many potential options.
W21	Inserted	Not inserted	
W22	Inserted	Not inserted	
W23	Inserted	Not inserted	
W24	Not inserted		
W25	Not populated		Not populated

The hardware that can be reconfigured falls into one of the following sections:

- ❑ Jumpers
- ❑ Switches
- ❑ Connectors

2.2 Jumpers

The table below lists the functions that users can reconfigure along with the shipping condition.

Table 2–3. Jumper/Function Reference

Function	Reference Designator	Subsection
Channel 0		
Analog input	W1, W11, W4, W2, W3	3.2.3
Analog output	W14, W19, W18	3.2.4
Disable onboard signal generator	W9	3.2.7
Voltage reference	W16, W17	3.2.8
3.3-V/5-V analog supply select	W13	3.2.9
Clock/timer routing	W20, W21, W22, W23, W24	3.2.10

2.2.1 Analog I/O Signal Conditioning

The TLC4541 supports various signal conditioning configurations.

The user has the following options:

- ❏ Bypass signal conditioning
- ❏ Use the onboard signal conditioning. This consists of an operational amplifier for each input channel configured with a gain of 1.
- ❏ Use the prototype area for signal conditioning.
- ❏ Use the expansion connector via a TI universal operational amplifier evaluation module (such as SLOP224/SLOP249).

2.2.2 Channel 0 Analog Input

This is the primary analog input and can always be connected externally.

Analog Input Configuration Channel 0	
Reference Designator	**Functional Description**
W1	W1 allows the user to select between an analog input via BNC – J1 or IDC – J4 pin 1.
W11	W11 allows selection of either the conditioned or nonconditioned analog input signal.
W4	W4 allows the user to select either the prototype area output or the output from W11.
W2	W2 enables the user to select either the output from the expansion connector or the output from the onboard signal generator.
W3	W3 completes the selection choices for channel 0 by determining if the output from W2 or W4 is chosen to be presented to the ADC.

2.2.3 Channel 0 Analog Output

With a one-channel DAC installed, this signal is the primary analog output (output A).

With a two-channel DAC installed, the pinout of these devices effectively resolves this channel to be the secondary analog output (output B).

Analog Input Configuration Channel 0	
Reference Designator	**Functional Description**
W19	This jumper selects the source for the analog output on channel 0. When a jumper is installed between pins 1 and 2, the output from the expansion connector's B-channel is routed out. When the jumper is installed between pins 2 and 3, the output from the onboard signal conditioning is directed through channel 0.

2.2.4 Signal Generator

Signal Generator	
Reference Designator	**Functional Description**
W9	W9 controls the generation of both onboard test signals. A jumper installed between pins 1 and 2 disables the waveform generator.

2.2.5 Voltage Reference

Voltage Reference	
Reference Designator	**Functional Description**
W16	W16 selects either the onboard reference or an external reference supplied by the user.
W17	W17 allows the user to vary the reference voltage.
W14	There are a number of possible DACs that a user can install on this EVM. Some have an internal reference that the user can select via software, and some do not have an internal reference. For the DACs that support an internal reference, it is important to have the facility to remove the external reference supplied by the EVM (or user) to avoid conflicts between the DAC's internal reference and the external reference.

2.2.6 ADC Supply Voltage

ADC Supply Voltage	
Reference Designator	**Functional Description**
W13	This jumper controls the analog supply voltage. When the jumper is installed, the supply voltage to the ADC is 3.3 V. When the jumper is not installed, the supply voltage to the ADC is 5 V.

2.2.7 Clock/Timer Routing

A variety of options are available to the user. Be careful about altering these.

Clock/Timer Routing	
Reference Designator	**Functional Description**
W21	This jumper defines the clock that the ADC and DAC use for all their timing. The user can select either the output from W23 or the output from W22 to be the base clock for the system.
W23	This jumper allows the user to select either an external clock, or the onboard 20-MHz oscillator for conversion. In addition, this signal is fed to W20.
W20	W20 provides a route for the EVM to generate CLKS for a DSP if so desired.
W22	This jumper enables the user to select either the transmit clock from a DSP, or the output from W24.
W24	W24 connects or isolates the timer output from a DSP.

2.3 Switches

There are three switches present on the EVM:

- One 8-pin DIL switch which houses four individual switches; these are denoted SW1-1, SW1-2, SW1-3, and SW1-4.
- Two momentary push-button switches

Features and functions of each switch:

Reference Designator	Function	Default Condition
SW1-1	Selects either stand-alone mode (SAM) or user mode	SAM
SW1-2	Reserved	
SW1-3	Reserved	
SW1-4	Reserved	

2.3.1 Stand-Alone-Mode, SW1-1

SW1-1 chooses either stand-alone mode or user mode. If the switch is set to the off position, SAM is selected and the EVM ignores all signals generated by a DSP. In addition, the EVM will not output any signals to a DSP or microprocessor.

In this mode, SW2 and SW3 are used to reset the EVM's logic and initiate automatic conversions from the ADC, in addition to automatically routing the serial bit stream from the ADC to the DAC for reconstruction.

Reference Designator	Function
SW2	Initiates ADC and DAC conversions in SAM
SW3	Forces the EVM's control logic into a known state

If SW1-1 is set to the on position, user mode is selected. In this case the user has absolute control of the data and control signals for the ADC and DAC. With SW1-1 in the on position, the logic that generates the control for SAM is disabled and plays no active part in the process.

2.4 Connectors

In addition to jumpers and switches, the user also has access to various connectors. This section details the pinout of each connector.

Reference Designator	Description
J1	Analog input option for channel 0, miniature BNC

Cells in grey are not supported (tracked) directly by this EVM.

Reference Designator	Description	Pin Number	Function
J3	Analog input option for universal operational-amplifier evaluation board, SIL PTH not installed.	1	Noninverting input signal to dual operational amplifier, (2)
		2	Noninverting input signal to dual operational amplifier, (2)
		3	Inverting input signal to dual operational amplifier, (2)
		4	Inverting input signal to dual operational amplifier, (2)
		5	Nonfiltered output from dual operational amplifier, (2)
		6	Filtered output from dual operational amplifier, (2)
		7	+V supply
		8	Operational amplifier (2) shutdown signal
		9	Reference voltage
		10	Analog ground
		11	Operational amplifier (1) shutdown signal
		12	–V supply
		13	Nonfiltered output from dual operational amplifier, (1)
		14	Filtered output from dual operational amplifier, (1)
		15	Noninverting input signal to dual operational amplifier, (1)
		16	Noninverting input signal to dual operational amplifier, (1)
		17	Inverting input signal to dual operational amplifier, (1)
		18	Inverting input signal to dual operational amplifier, (1)

Reference Designator	Description	Pin Number	Function
J4	Analog input option, 26-pin DIL header	1	Channel 0 input
		2	AGND
		3	Channel 1 input
		4	AGND
		5	Not connected
		6	AGND
		7	Not connected
		8	AGND
		9	Not connected
		10	AGND
		11	Not connected
		12	AGND
		13	Not connected
		14	AGND
		15	Not connected
		16	AGND
		17	Not connected
		18	AGND
		19	Not connected
		20	AGND
		21	Not connected
		22	AGND
		23	Not connected
		24	AGND
		25	External reference voltage
		26	AGND

Reference Designator	Description
J5	Analog output for one-channel DAC

Reference Designator	Description	Pin Number	Function
J7	EVM power	1	5 V
		2	–12 V
		3	0 V
		4	12 V
J8	Analog output option, 26-pin DIL header	1	No output
		2	AGND
		3	Analog output for one-channel DAC
		4	AGND
		5	Not connected
		6	AGND
		7	Not connected
		8	AGND
		9	Not connected
		10	AGND
		11	Not connected
		12	AGND
		13	Not connected
		14	AGND
		15	Not connected
		16	AGND
		17	Not connected
		18	AGND
		19	Not connected
		20	AGND
		21	Not connected
		22	AGND
		23	Not connected
		24	AGND
		25	Not connected
		26	AGND

Reference Designator	Description	Pin Number	Function
J9	Analog input option for universal operational-amplifier evaluation board, SIL PTH not installed.	1	Noninverting input signal to dual operational amplifier, (2)
		2	Noninverting input signal to dual operational amplifier, (2)
		3	Inverting input signal to dual operational amplifier, (2)
		4	Inverting input signal to dual operational amplifier, (2)
		5	Nonfiltered output from dual operational amplifier, (2)
		6	Filtered output from dual operational amplifier, (2)
		7	+V supply
		8	Operational amplifier (2) shutdown signal
		9	Reference voltage
		10	Analog ground
		11	Operational amplifier (1) shutdown signal
		12	–V supply
		13	Nonfiltered output from dual operational amplifier, (1)
		14	Filtered output from dual operational amplifier, (1)
		15	Noninverting input signal to dual operational amplifier, (1)
		16	Noninverting input signal to dual operational amplifier, (1)
		17	Inverting input signal to dual operational amplifier, (1)
		18	Inverting input signal to dual operational amplifier, (1)

2.5 ADC and DAC Direct Access

J10 and J11 offer users the facility to directly inspect the digital signals coming from and going to the ADC and DAC.

Reference Designator	Description	Pin Number	Signal
J10	Allows the user direct access to all digital signals for the ADC	1	Digital ground
		2	SDO
		3	Digital ground
		4	SCLK
		5	Digital ground
		6	$\overline{CS}$ or $\overline{CS}$/FS
		7	Digital ground
		8	FS
J11	Allows the user direct access to all digital signals for the DAC	1	Digital ground
		2	SDI
		3	Digital ground
		4	SCLK
		5	Digital ground
		6	$\overline{CS}$
		7	Digital ground
		8	FS

2.6 Host Communication

There are two ways to connect a host system (DSP/microprocessor):

- Texas Instruments' new DSKs provide two dedicated 80-pin connectors. The EVM can be plugged directly onto these DSKs. This connector standard is referred to as the common connector.
- Legacy DSKs not equipped with the 80-pin common connectors will communicate via the daisy-chained legacy header.

The following sections discuss each connection method.

2.6.1 Common Connector

Reference Designator	Description	Pin Number	Function
J16	80-pin memory interface connector for ’C5000 and ’C6000 DSK EVMs. Pins unused by this EVM are omitted for clarity.	1	5 V
		2	5 V
		11	PCI ground
		12	PCI ground
		21	5 V
		22	5 V
		29	PCI ground
		30	PCI ground
		31	PCI ground
		32	PCI ground
		41	3.3 V
		42	3.3 V
		51	PCI ground
		52	PCI ground
		61	PCI ground
		62	PCI ground
		71	PCI ground
		72	PCI ground
		79	PCI ground
		80	PCI ground

Reference Designator	Description	Pin Number	Function
J17	80-pin peripheral and control connector for ’C5000 and ’C6000 DSK EVMs. Pins unused by this EVM are omitted for clarity.	1	12 V
		2	–12 V
		3	PCI ground
		4	PCI ground
		5	5 V
		6	5 V
		7	PCI ground
		8	PCI ground
		9	5 V
		10	5 V
		35	FSX
		33	CLKX
		36	DX
		25	PCI ground
		26	PCI ground
		39	CLKR
		41	FSR
		42	DR
		31	PCI ground
		32	PCI ground
		37	PCI ground
		38	PCI ground
		43	PCI ground
		44	PCI ground
		45	TOUT
		49	XF
		51	PCI ground
		52	PCI ground
		61	PCI ground
		62	PCI ground
		76	PCI ground
		77	PCI ground
		79	PCI ground
		80	PCI ground

2.6.2 Legacy Connector

J12, J13, and J15 are three 2x20 headers daisy-chained together and are collectively referred to as the legacy connector. The principle behind this arrangement is to eliminate the confused and untidy custom cabling that is typically present when connecting a legacy DSP to an EVM. This daisy-chained connector method is flexible, robust, and makes it possible to use a standard flat signal-cable assembly, improving reliability of communications between host and EVM.

Two shorting bars are inserted in J12 and J15; these bars permit alternate pins on J13 to be DGND. If the user has complete discretion over signal routing at the host end, it is recommended that the host-end connector should reflect the same pinout as J13.

However, if the host-end connector does not (or cannot) mirror the pinout for J13, then some degree of signal-twisting is necessary. This is accomplished on the EVM by removing the shorting bars on J12 and J15 and typically wire-wrapping directly onto the appropriate header.

For example, if the host connector on the DSP has the pin assignment described in the following table, then a 1:1 mapping is possible and the user should plug a flat 20-way ribbon cable into J13.

Host Connector				EVM Connector – J13			
Pin No.	**Signal**	**Pin No.**	**Signal**	**Pin No.**	**Signal**	**Pin No.**	**Signal**
1	XF	2	DGND	1	XF	2	DGND
3	CLKX	4	DGND	3	CLKX	4	DGND
5	CLKR	6	DGND	5	CLKR	6	DGND
7	DX	8	DGND	7	DX	8	DGND
9	DR	10	DGND	9	DR	10	DGND
11	FSX	12	DGND	11	FSX	12	DGND
13	FSR	14	DGND	13	FSR	14	DGND
15	Resvd	16	DGND	15	Resvd	16	DGND
17	CLKS	18	DGND	17	CLKS	18	DGND
19	TOUT	20	DGND	19	TOUT	20	DGND

However, if the host connector has a different signal pinout, the user should remove the shorting bars from J12 and J15. A flat 20-way IDC ribbon cable can still be used; in this case, the user should plug the connector into J12 of the EVM. Since the cable is now plugged into J12, and all the signals on both sides of the J12 pins are routed to adjacent connector pins (J13 and J15), the user can typically wire-wrap the associated host signal to the relevant EVM signal.

The example shown below demonstrates the steps that must be taken to reassign the connector and wire-wrap the correct signals.

Consider a host cable signal assignment as shown below:

Host Connector			
Pin No.	**Signal**	**Pin No.**	**Signal**
1	NA	2	DGND
3	NA	4	DGND
5	CLKX	6	CLKR
7	TOUT	8	DGND
9	DX	10	DR
11	FSX	12	FSR
13	NA	14	DGND
15	XF	16	DGND
17	NA	18	NA
19	NA	20	CLKS

The host connector mates with J12. Signals on either side of J12 are available on J13 and J15.

J13	Host Connector Plugged into J12				J15
Pin No.	**Pin No.**	**Signal**	**Pin No.**	**Signal**	**Pin No.**
2	1	N/A	2	DGND	1
4	3	N/A	4	DGND	3
6	5	CLKX	6	CLKR	5
8	7	TOUT	8	DGND	7
10	9	DX	10	DR	9
12	11	FSX	12	FSR	11
14	13	N/A	14	DGND	13
16	15	XF	16	DGND	15
18	17	N/A	18	N/A	17
20	19	N/A	20	CLKS	19

For clarity, the above table can be redrawn with J12 removed.

J13		J15	
Pin No.	**Signal**	**Pin No.**	**Signal**
2	NA	1	DGND
4	NA	3	DGND
6	CLKX	5	CLKR
8	TOUT	7	DGND
10	DX	9	DR
12	FSX	11	FSR
14	NA	13	DGND
16	XF	15	DGND
18	NA	17	NA
20	NA	19	CLKS

The table below shows the signal names and pin assignments that the composite connector shown above must be mapped onto.

J13	
Pin No.	**Signal**
1	XF
3	CLKX
5	CLKR
7	DX
9	DR
11	FSX
13	FSR
15	Resvd
17	CLKS
19	TOUT

All of the signals required to interface the EVM to the host are now available on either J13 or J15. This is simply a matter of wire-wrapping in the following way:

J13		Wire Wrap	J13	
Pin No.	**Signal**		**Pin No.**	**Signal**
2	NA			
4	NA			
6	CLKX		3	CLKX
8	TOUT		19	TOUT
10	DX		7	DX
12	FSX		11	FSX
14	NA			
16	XF		1	XF
18	NA			
20	NA			

J15		Wire Wrap	J13		Jumper Between	J15	
Pin No.	**Signal**		**Pin No.**	**Signal**		**Pin No.**	**Signal**
1	DGND				YES	2	DGND
3	DGND				YES	4	DGND
5	CLKR	YES	5	CLKR		6	DGND
7	DGND				YES	8	DGND
9	DR	YES	9	DR		10	DGND
11	FSR	YES	13	FSR		12	DGND
13	DGND				YES	14	DGND
15	DGND				YES	16	DGND
17	NA					18	DGND
19	CLKS	YES	17	CLKS		20	DGND

All of these connectors are shown below:

Reference Designator	Description	Pin Number	Signal Name/Function
J12	20-pin connector	1	J13 pin 2
		2	J15 pin 1
		3	J13 pin 4
		4	J15 pin 3
		5	J13 pin 6
		6	J15 pin 5
		7	J13 pin 8
		8	J15 pin 7
		9	J13 pin 10
		10	J15 pin 9
		11	J13 pin 12
		12	J15 pin 11
		13	J13 pin 14
		14	J15 pin 13
		15	J13 pin 16
		16	J15 pin 15
		17	J13 pin 18
		18	J15 pin 17
		19	J13 pin 20
		20	J15 pin 19

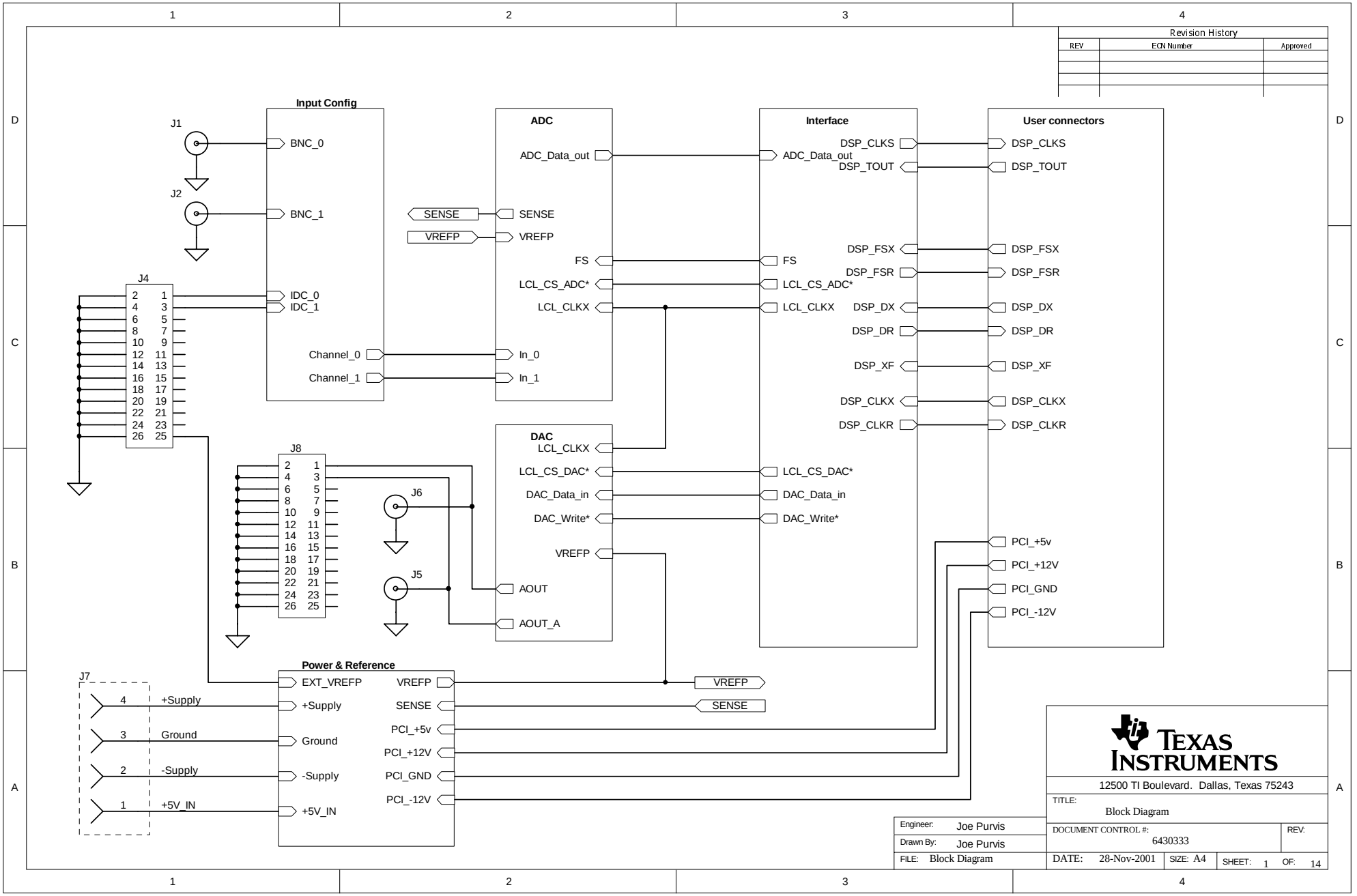
Reference Designator	Description	Pin Number	Signal Name/Function
J13	20-pin signal connector	1	ADC select signal
		2	J12 pin 1
		3	CLKX/transmit clock
		4	J12 pin 3
		5	CLKR receive clock
		6	J12 pin 5
		7	DX/data transmit
		8	J12 pin 7
		9	DR/data receive
		10	J12 pin 9
		11	FSX/frame sync transmit
		12	J12 pin 11
		13	FSR/frame sync receive
		14	J12 pin 13
		15	Reserved
		16	J12 pin 15
		17	CLKS/sync clock
		18	J12 pin 17
		19	TOUT/host timer output
		20	J12 pin 19

Reference Designator	Description	Pin Number	Signal Name/Function
J15	20-Pin connector	1	J12 pin 2
		2	DGND
		3	J12 pin 4
		4	DGND
		5	J12 pin 6
		6	DGND
		7	J12 pin 8
		8	DGND
		9	J12 pin 10
		10	DGND
		11	J12 pin 12
		12	DGND
		13	J12 pin 14
		14	DGND
		15	J12 pin 16
		16	DGND
		17	J12 pin 18
		18	DGND
		19	J12 pin 20
		20	DGND

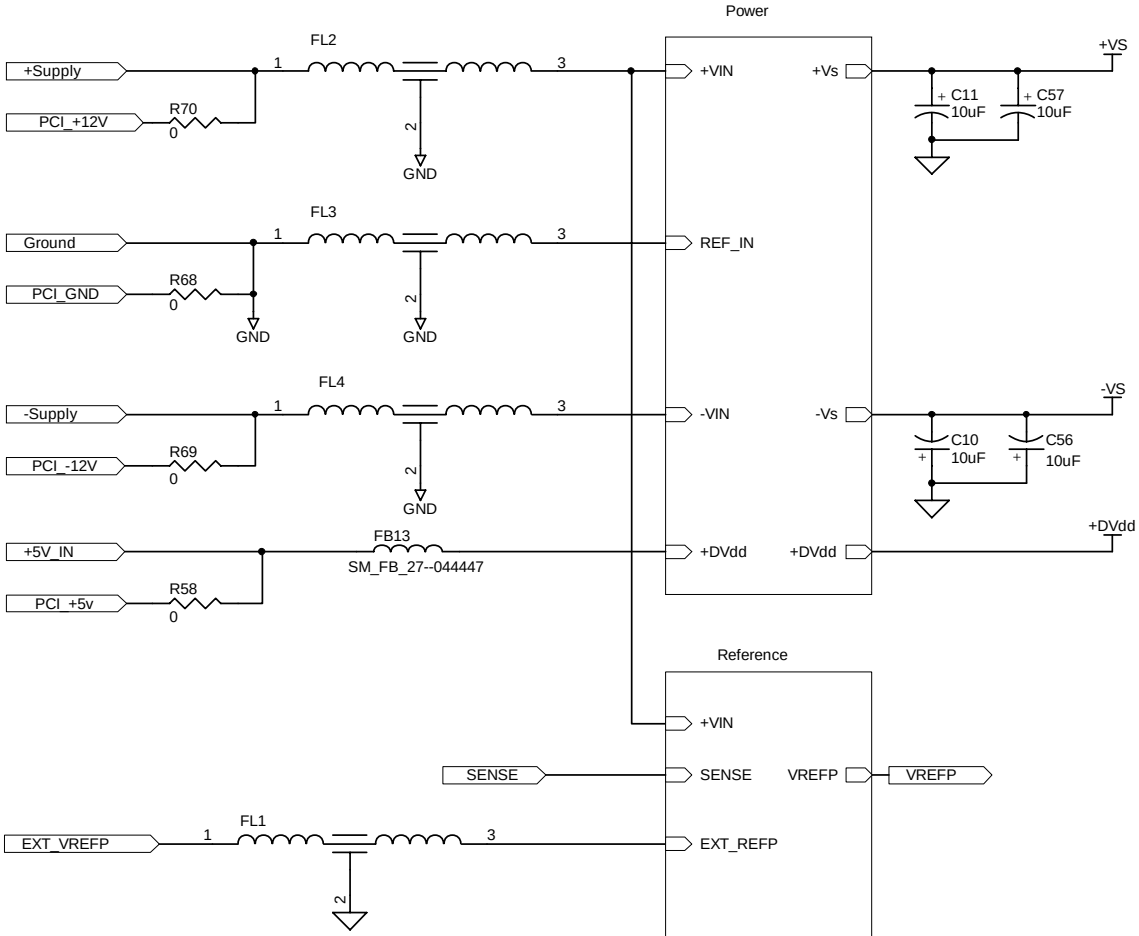
Appendix A

Bill of Materials, Board Layout, and Schematics

This appendix contains the bill of materials, board layouts, and the EVM schematics.


Revision History
REV
ECN Number
Approved
Input Config
ADC
Interface
User connectors
J1
J2
BNC_0
BNC_1
SENSE
VREFP
ADC_Data_out
FS
LCL_CS_ADC*
LCL_CLKX
Channel_0
Channel_1
In_0
In_1
DSP_CLKS
DSP_TOUT
DSP_FSX
DSP_FSR
DSP_DX
DSP_DR
DSP_XF
DSP_CLKX
DSP_CLKR
J4
IDC_0
IDC_1
J8
DAC
LCL_CS_DAC*
DAC_Data_in
DAC_Write*
J6
J5
AOUT
AOUT_A
PCI_+5v
PCI_+12V
PCI_GND
PCI_-12V
J7
4
3
2
1
+Supply
Ground
-Supply
+5V_IN
Power & Reference
EXT_VREFP
Texas Instruments
12500 TI Boulevard. Dallas, Texas 75243
TITLE:
Block Diagram
DOCUMENT CONTROL #:
6430333
REV:
Engineer: Joe Purvis
Drawn By: Joe Purvis
FILE: Block Diagram
DATE: 28-Nov-2001
SIZE: A4
SHEET: 1
OF: 14

Revision History		
REV	ECN Number	Approved
2	040500	



Engineer:	Joe Purvis
Drawn By:	Joe Purvis
FILE:	Power & Reference

TEXAS INSTRUMENTS

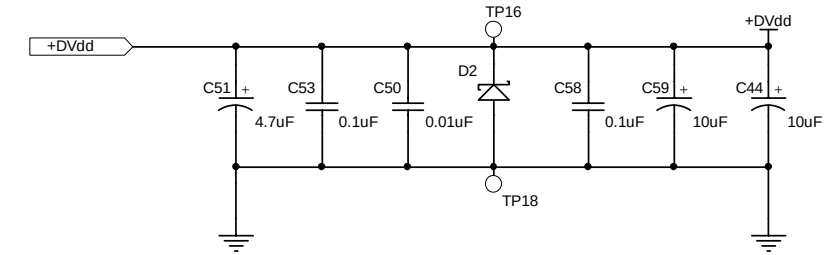
12500 TI Boulevard. Dallas, Texas 75243

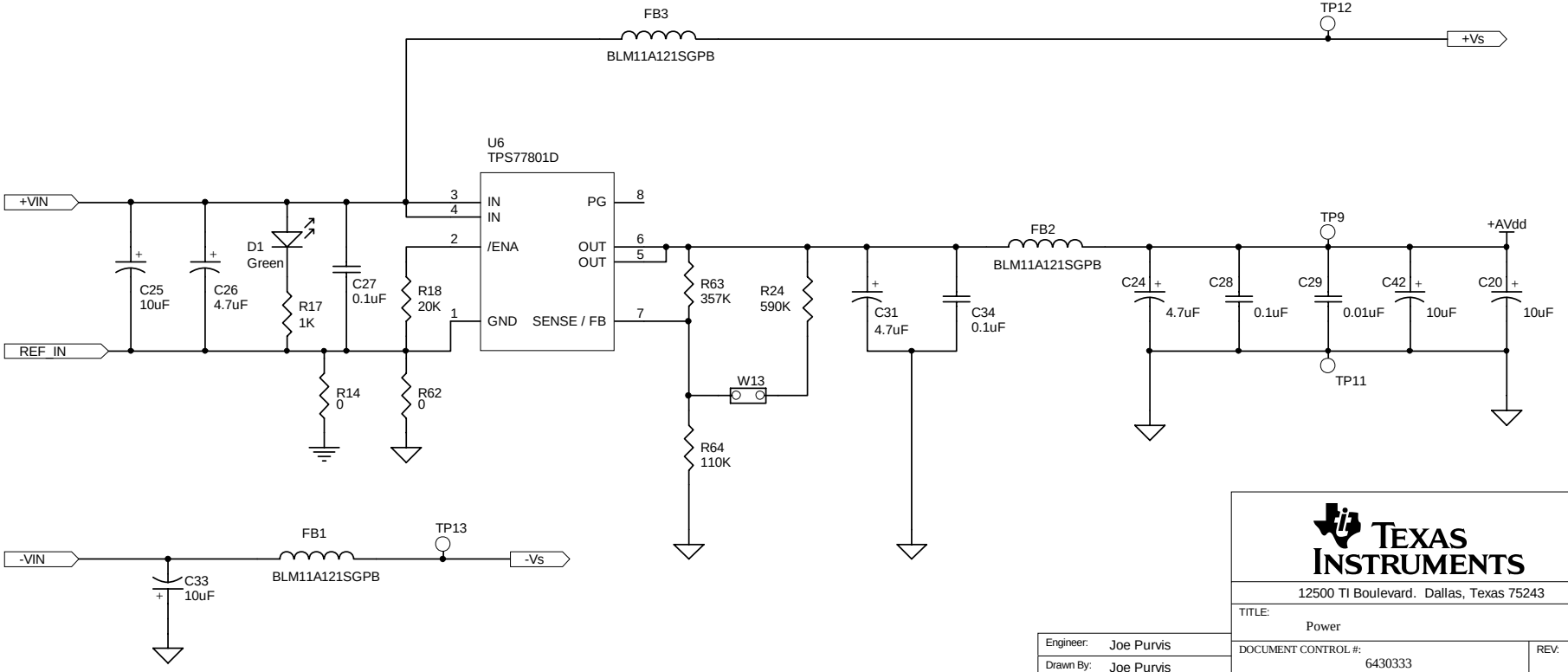
TITLE: Power & Reference

DOCUMENT CONTROL #: 6430333 REV:

DATE: 28-Nov-2001 SIZE: A4 SHEET: 2 OF: 14

Revision History		
REV	ECN Number	Approved
F	040500	





Engineer:	Joe Purvis
Drawn By:	Joe Purvis
FILE:	Power

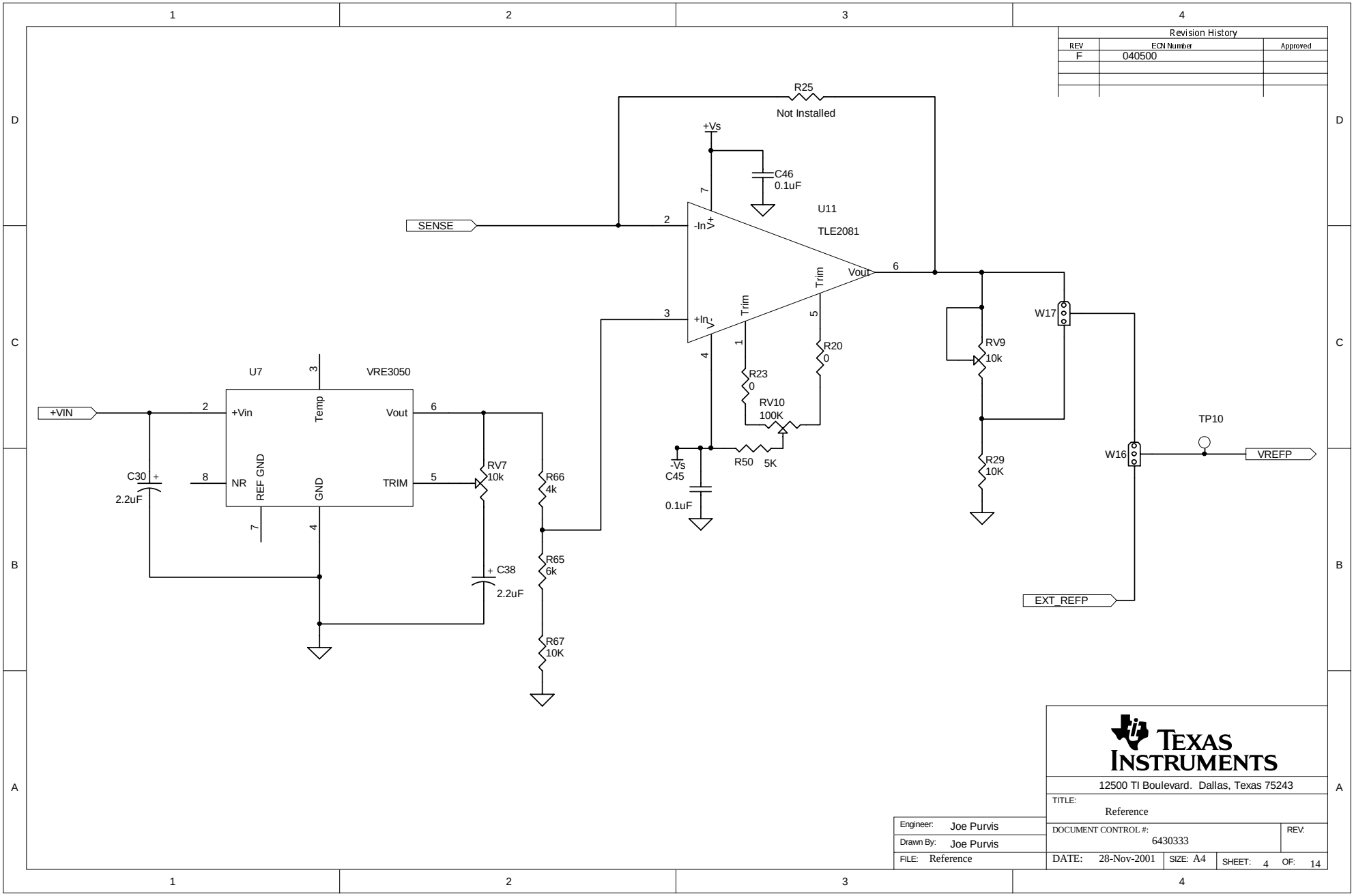
TEXAS INSTRUMENTS

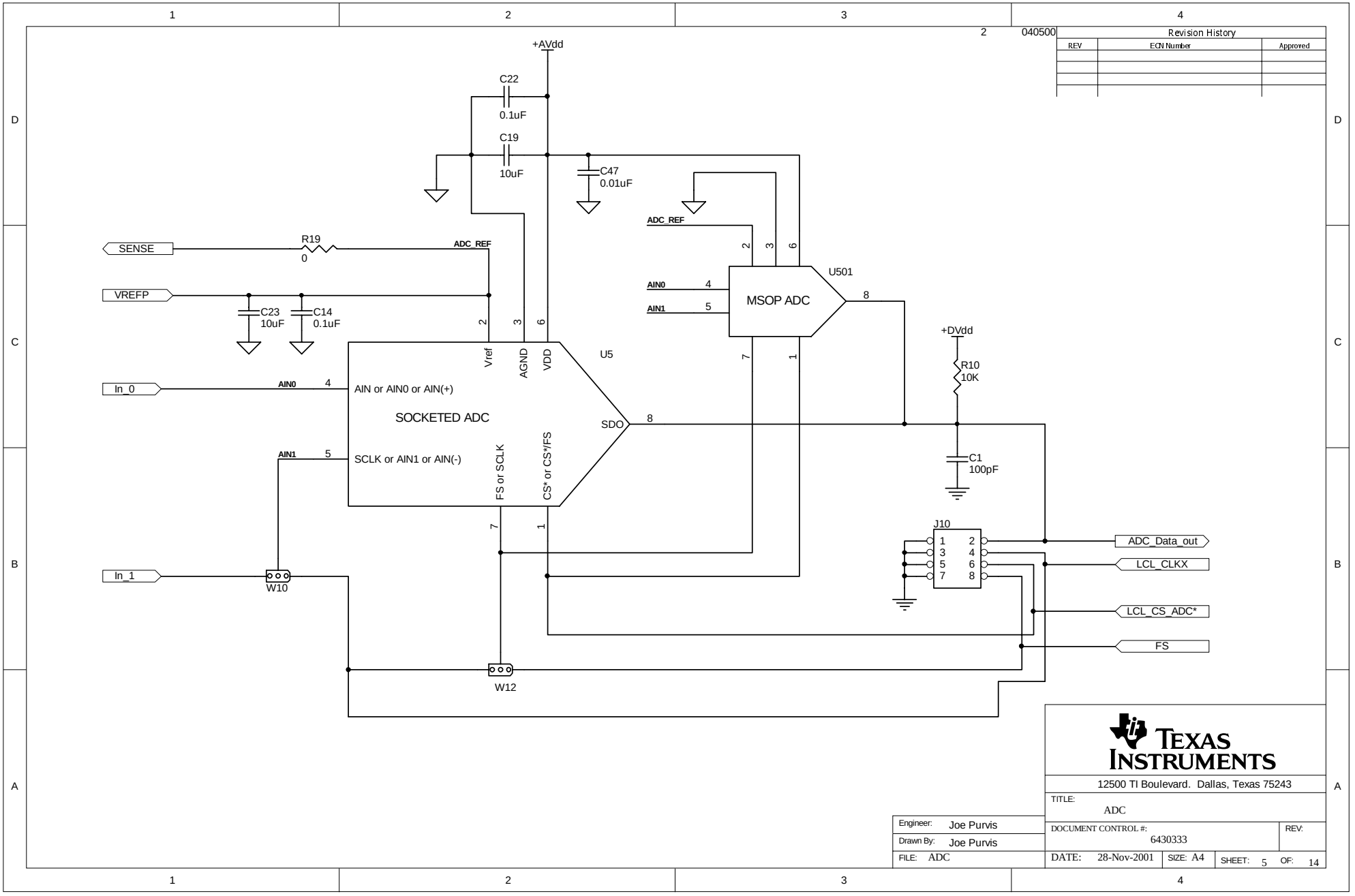
12500 TI Boulevard. Dallas, Texas 75243

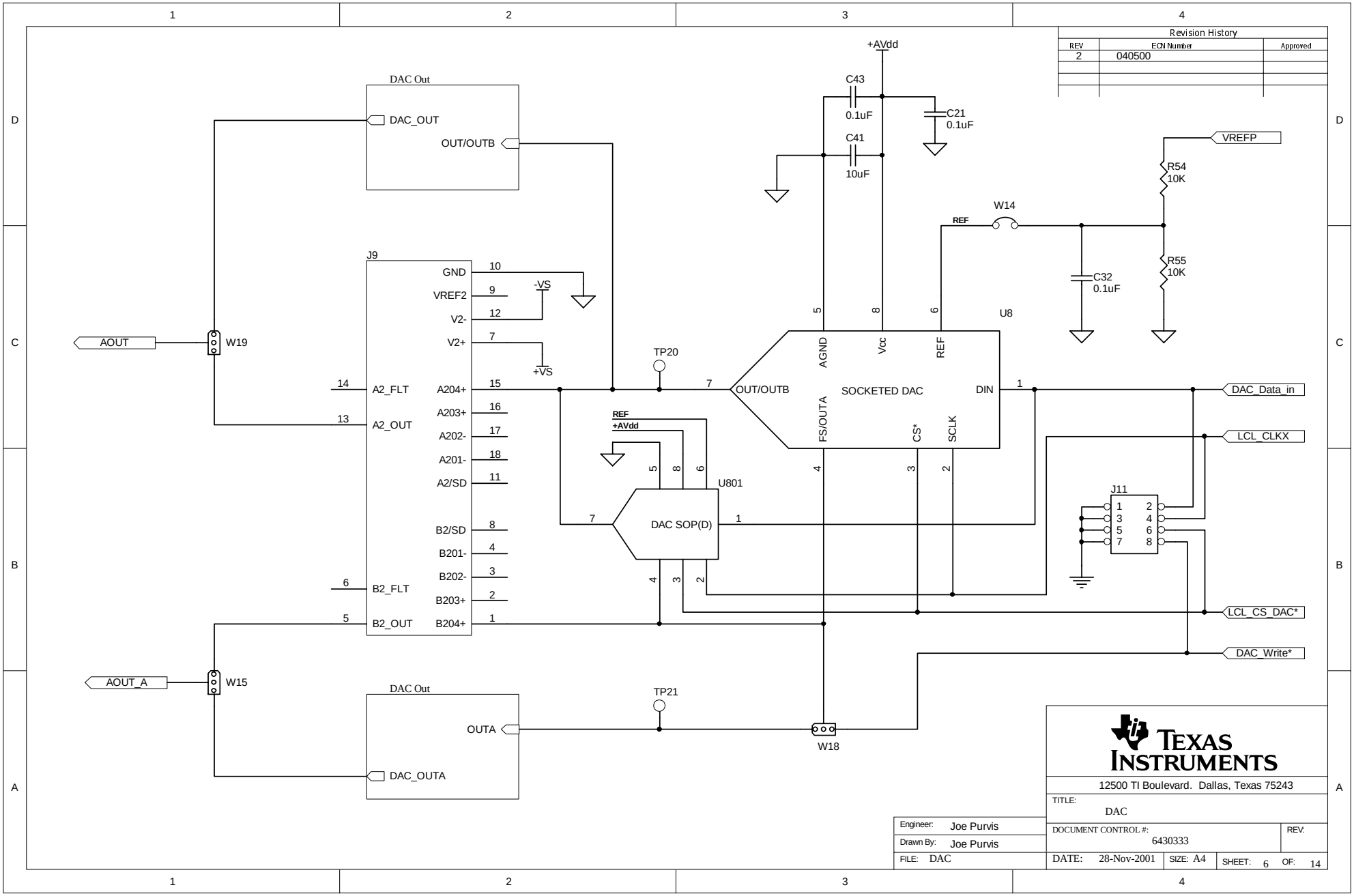
TITLE: Power

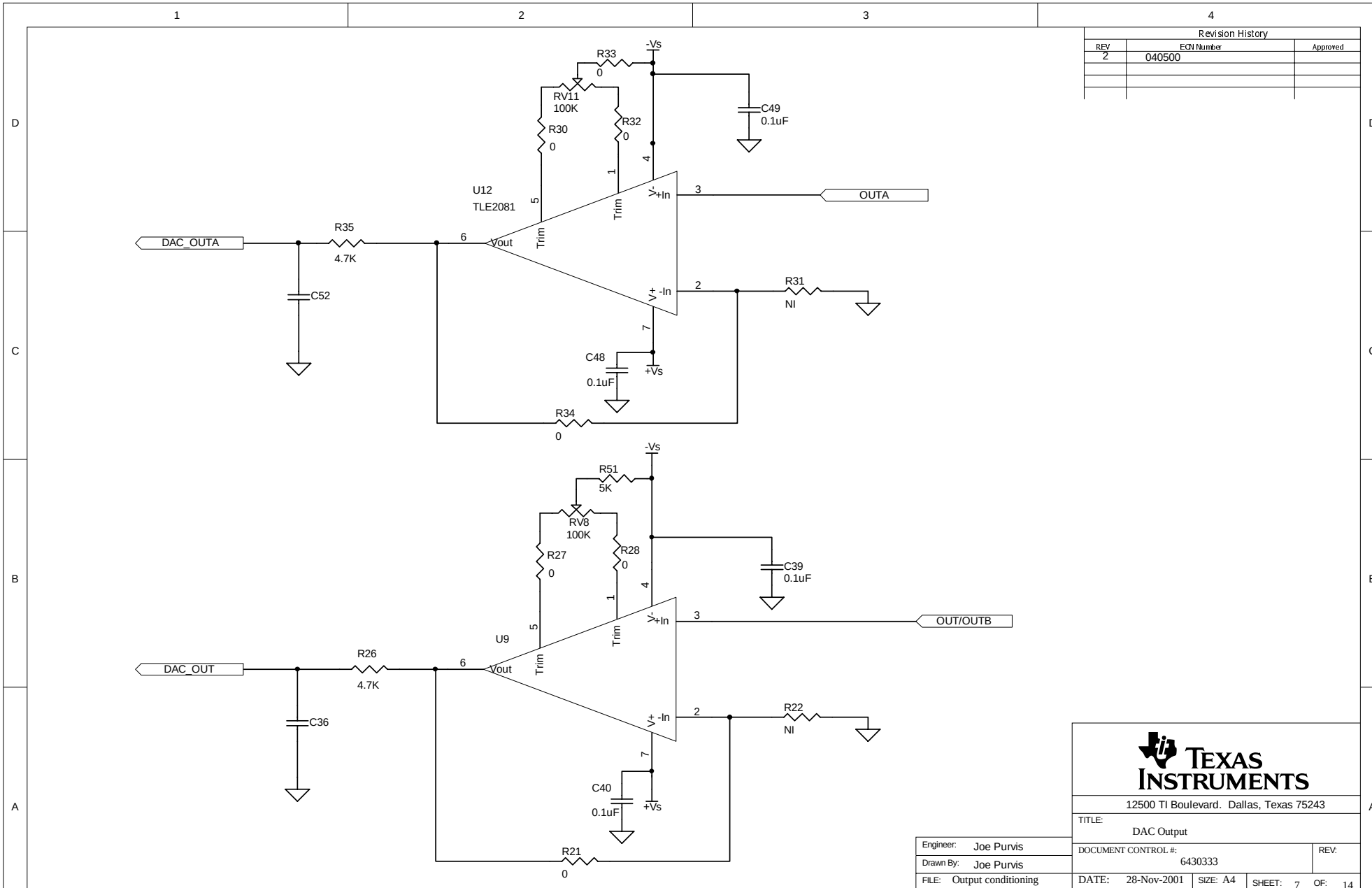
DOCUMENT CONTROL #: 6430333 REV:

DATE: 28-Nov-2001 SIZE: A4 SHEET: 3 OF: 14

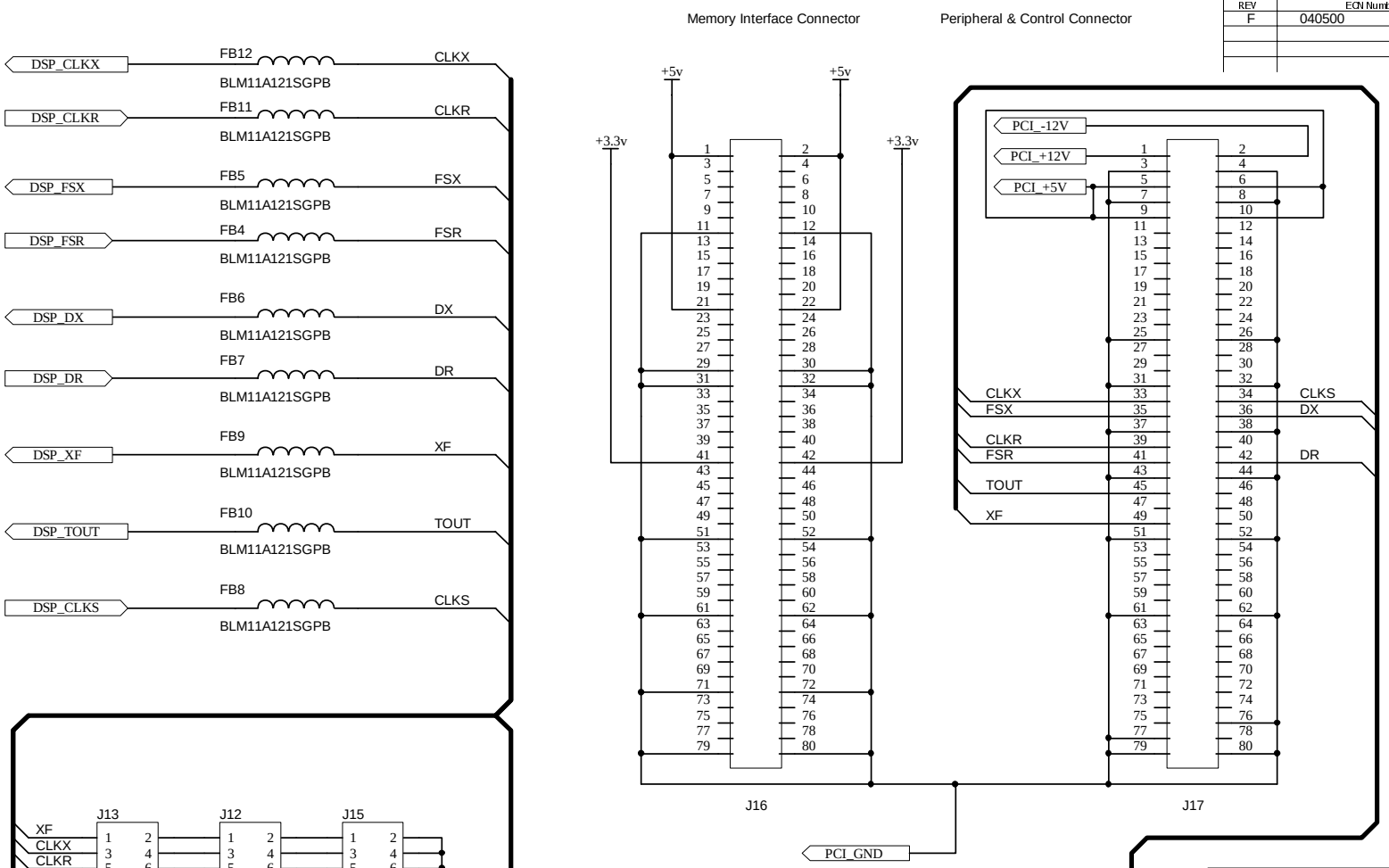

Revision History
REV
ECN Number
Approved
F
040500
R25
Not Installed
+Vs
C46
0.1uF
U11
TLE2081
SENSE
-In
+In
Vout
Trim
R20
0
R23
0
RV10
100K
R50
5K
-Vs
C45
0.1uF
RV9
10k
W17
R29
10K
W16
TP10
VREFP
EXT_REFP
U7
VRE3050
+VIN
+Vin
Temp
Vout
NR
REF GND
GND
TRIM
C30
2.2uF
RV7
10k
R66
4k
R65
6k
C38
2.2uF
R67
10K
TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243
TITLE:
Reference
DOCUMENT CONTROL #:
6430333
REV:
Engineer: Joe Purvis
Drawn By: Joe Purvis
FILE: Reference
DATE: 28-Nov-2001
SIZE: A4
SHEET: 4
OF: 14


2
040500
Revision History
REV
ECN Number
Approved
+AVdd
C22
0.1uF
C19
10uF
C47
0.01uF
ADC_REF
SENSE
R19
0
VREFP
C23
10uF
C14
0.1uF
U501
MSOP ADC
AIN0
AIN1
+DVdd
R10
10K
U5
Vref
AGND
VDD
SOCKETED ADC
AIN or AIN0 or AIN(+)
SCLK or AIN1 or AIN(-)
FS or SCLK
CS* or CS*/FS
SDO
C1
100pF
In_0
In_1
W10
W12
J10
ADC_Data_out
LCL_CLKX
LCL_CS_ADC*
FS
TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243
TITLE: ADC
DOCUMENT CONTROL #: 6430333
REV:
Engineer: Joe Purvis
Drawn By: Joe Purvis
FILE: ADC
DATE: 28-Nov-2001
SIZE: A4
SHEET: 5 OF: 14


Revision History
REV
ECN Number
Approved
2
040500
DAC Out
DAC_OUT
OUT/OUTB
+AVdd
C43
0.1uF
C21
0.1uF
C41
10uF
VREFP
R54
10K
W14
REF
R55
10K
C32
0.1uF
U8
AGND
Vcc
REF
SOCKETED DAC
OUT/OUTB
DIN
FS/OUTA
CS*
SCLK
J9
GND
VREF2
V2-
V2+
-VS
+VS
A2_FLT
A2_OUT
A204+
A203+
A202-
A201-
A2/SD
B2/SD
B201-
B202-
B203+
B204+
B2_FLT
B2_OUT
AOUT
W19
TP20
REF
+AVdd
U801
DAC SOP(D)
J11
DAC_Data_in
LCL_CLKX
LCL_CS_DAC*
DAC_Write*
AOUT_A
W15
DAC Out
OUTA
DAC_OUTA
TP21
W18
TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243
TITLE:
DAC
DOCUMENT CONTROL #:
6430333
REV:
Engineer: Joe Purvis
Drawn By: Joe Purvis
FILE: DAC
DATE: 28-Nov-2001
SIZE: A4
SHEET: 6
OF: 14


Revision History
REV
ECN Number
Approved
2
040500
-Vs
R33
0
RV11
100K
R30
0
R32
0
C49
0.1uF
U12
TLE2081
OUTA
R35
DAC_OUTA
4.7K
C52
Trim
Vout
V+ -In
R31
NI
C48
0.1uF
+Vs
R34
0
-Vs
R51
5K
RV8
100K
R27
0
R28
0
C39
0.1uF
U9
OUT/OUTB
R26
DAC_OUT
4.7K
C36
R22
NI
C40
0.1uF
+Vs
R21
0
TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243
TITLE:
DAC Output
DOCUMENT CONTROL #:
6430333
REV:
Engineer: Joe Purvis
Drawn By: Joe Purvis
FILE: Output conditioning
DATE: 28-Nov-2001
SIZE: A4
SHEET: 7 OF: 14

Revision History		
REV	ECN Number	Approved
F	040500	



Engineer:	Joe Purvis
Drawn By:	Joe Purvis
FILE:	User connectors

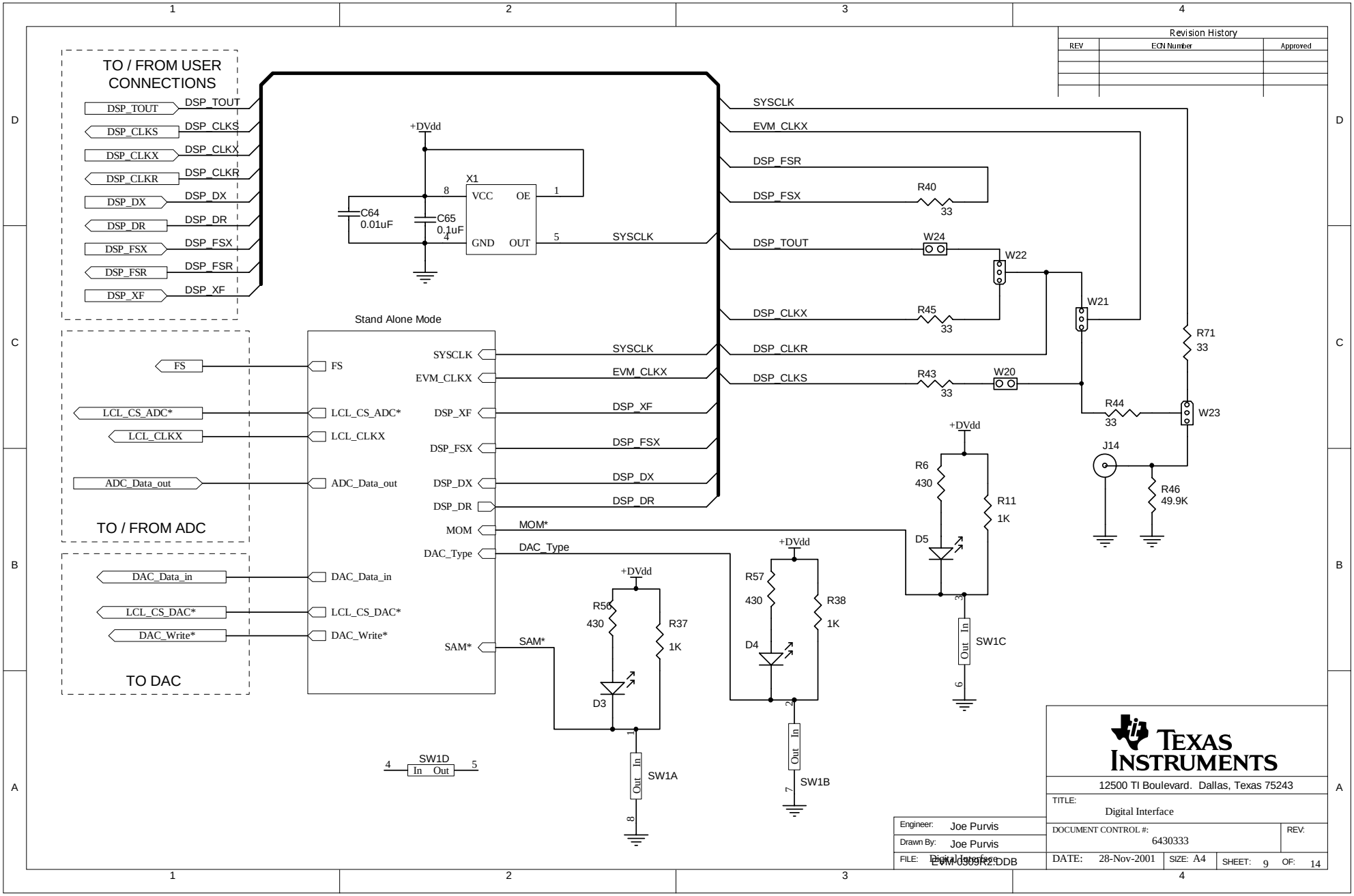
TEXAS INSTRUMENTS

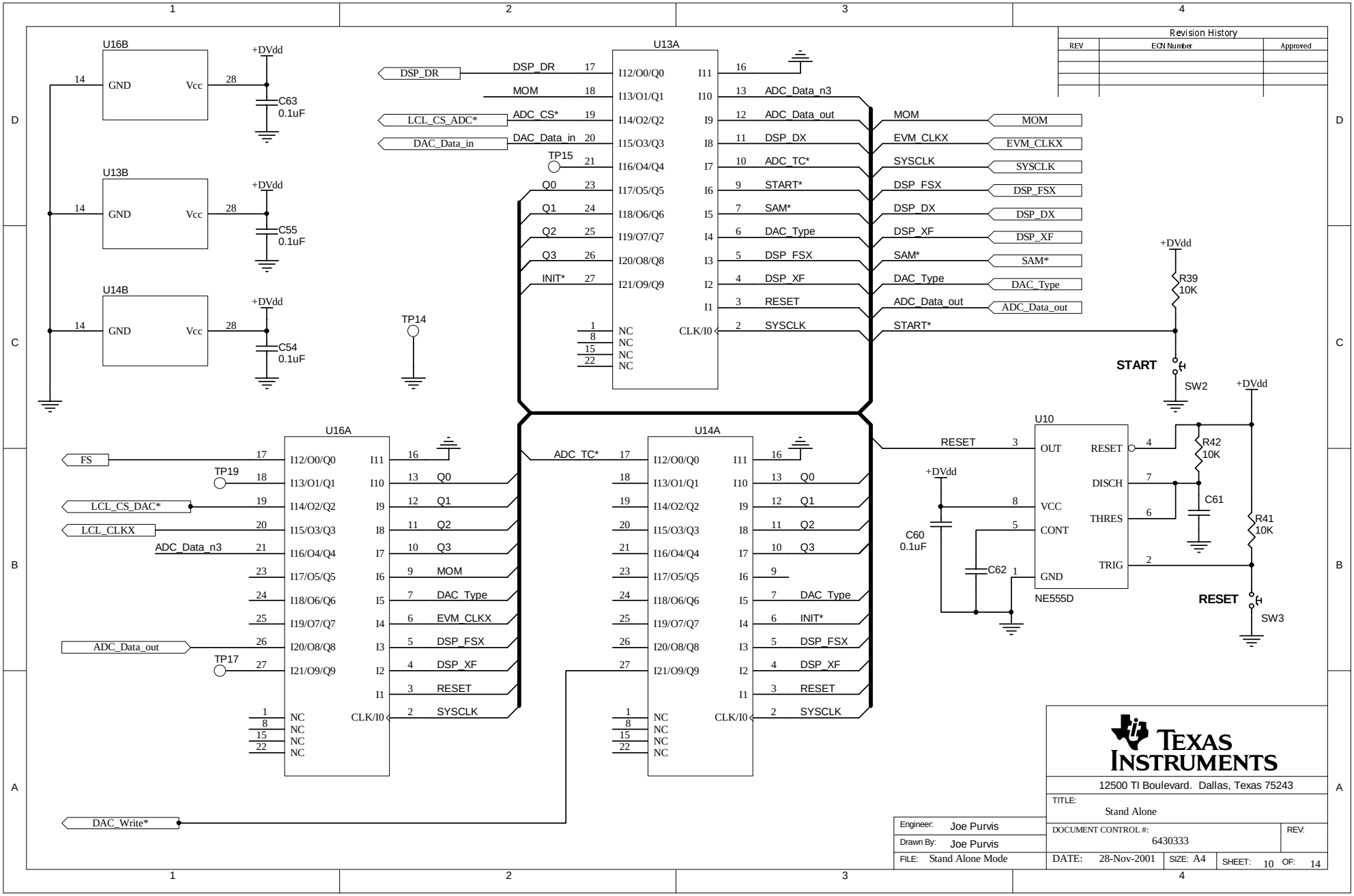
12500 TI Boulevard. Dallas, Texas 75243

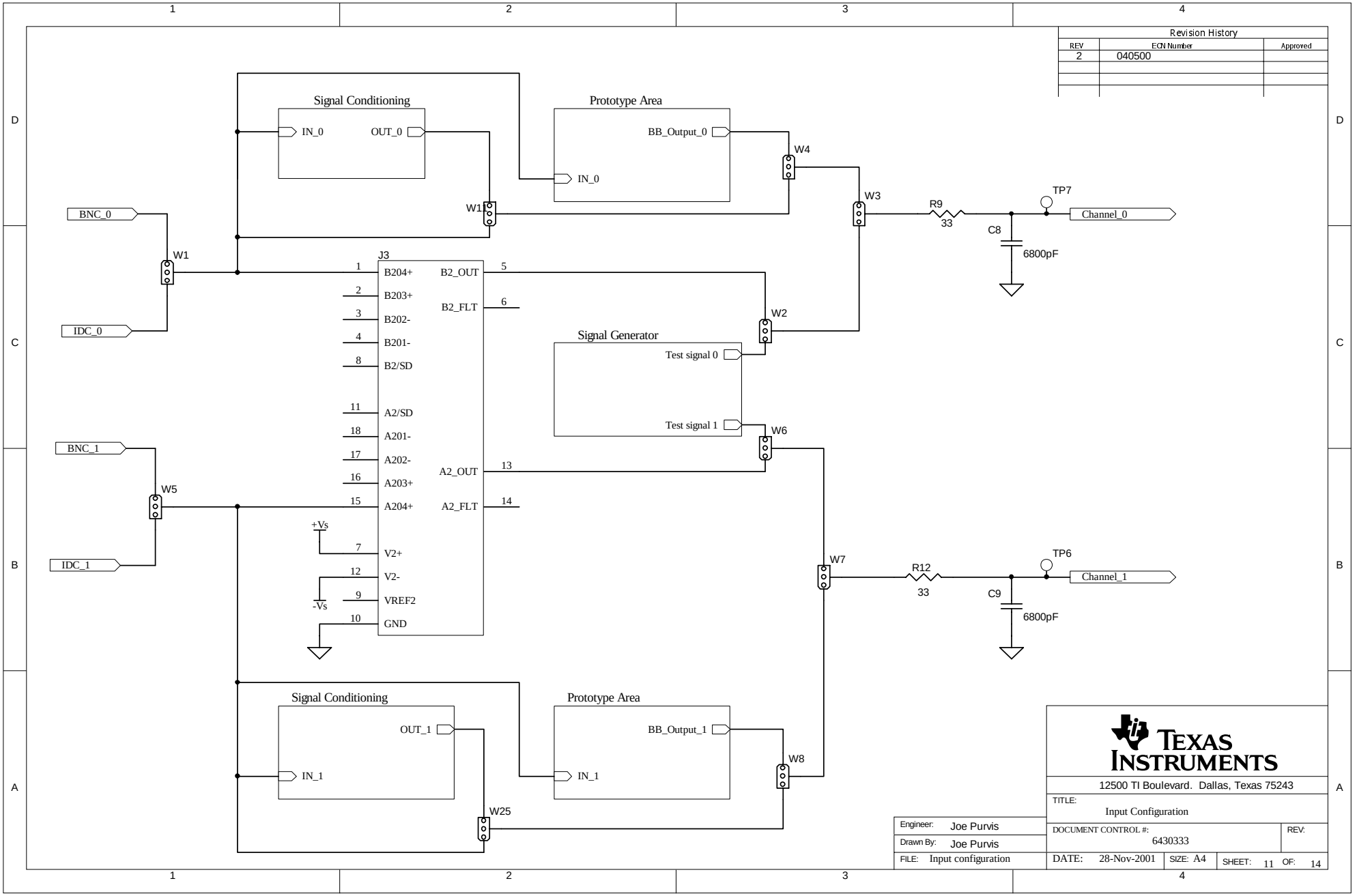
TITLE: User Connectors

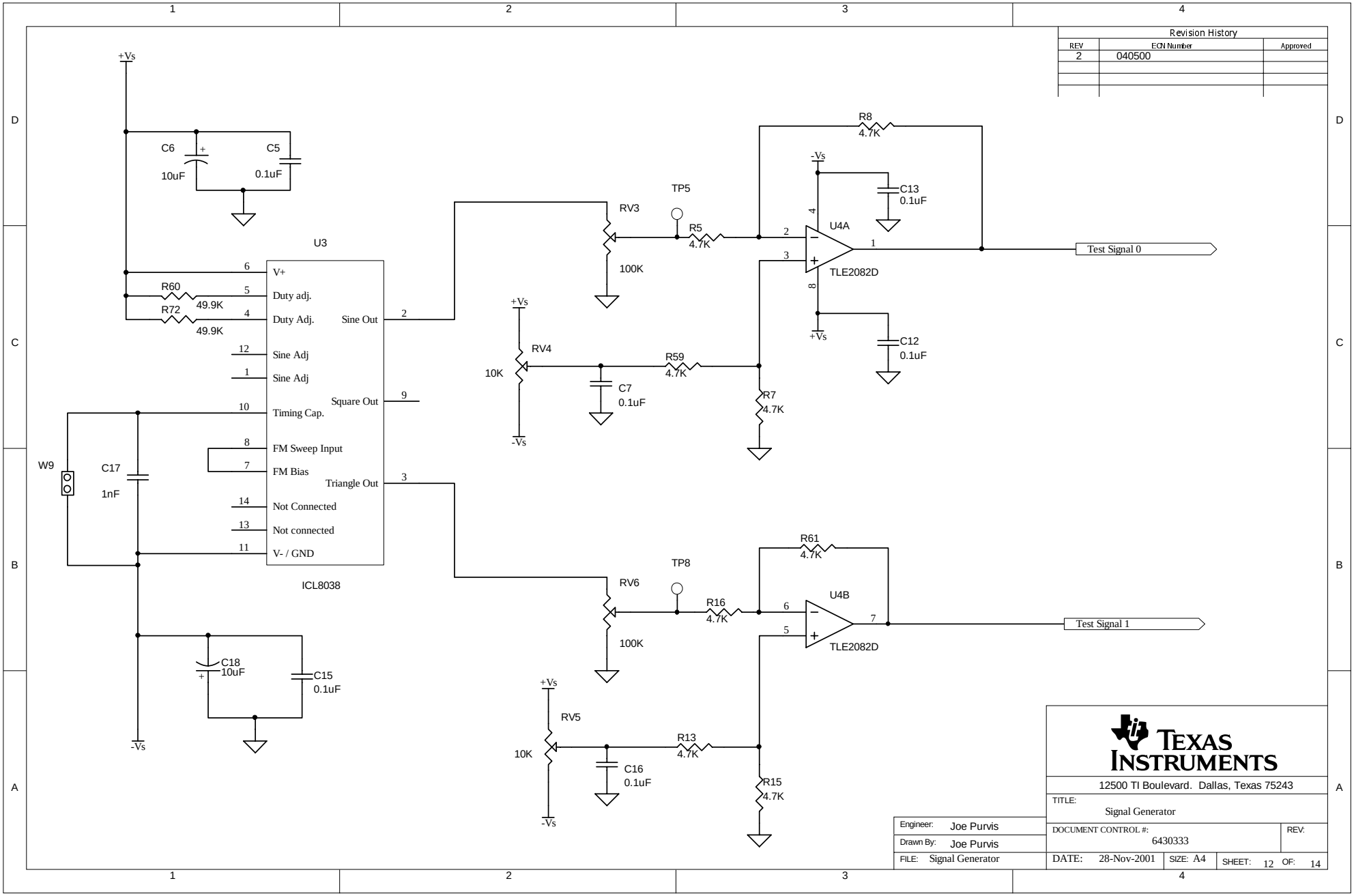
DOCUMENT CONTROL #: 6430333 REV:

DATE: 28-Nov-2001 SIZE: A4 SHEET: 8 OF: 14

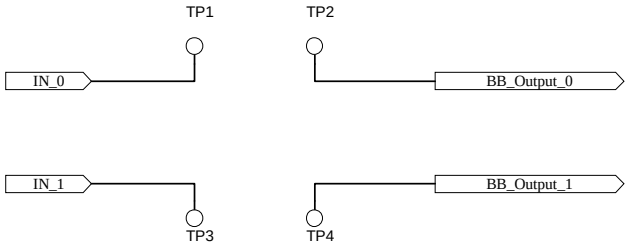

Revision History
REV
ECN Number
Approved
TO / FROM USER CONNECTIONS
DSP_TOUT
DSP_CLKS
DSP_CLKX
DSP_CLKR
DSP_DX
DSP_DR
DSP_FSX
DSP_FSR
DSP_XF
+DVdd
X1
VCC
OE
GND
OUT
C64
0.01uF
C65
0.1uF
SYSCLK
Stand Alone Mode
FS
LCL_CS_ADC*
LCL_CLKX
ADC_Data_out
TO / FROM ADC
DAC_Data_in
LCL_CS_DAC*
DAC_Write*
TO DAC
EVM_CLKX
DSP_XF
DSP_FSX
DSP_DX
DSP_DR
MOM
MOM*
DAC_Type
SAM*
R40
33
W24
W22
W21
R45
R71
R43
W20
R44
W23
J14
R46
49.9K
R6
430
R11
1K
D5
SW1C
Out In
R56
R37
D3
SW1A
R57
R38
D4
SW1B
SW1D
In Out
TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243
TITLE:
Digital Interface
DOCUMENT CONTROL #:
6430333
REV:
Engineer: Joe Purvis
Drawn By: Joe Purvis
FILE: Digital Interface
EVM-0309R2.DDB
DATE: 28-Nov-2001
SIZE: A4
SHEET: 9 OF: 14

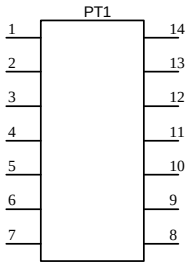

Revision History
REV
ECN Number
Approved
U16B
U13B
U14B
GND
Vcc
+DVdd
C63
0.1uF
C55
0.1uF
C54
0.1uF
U13A
U16A
U14A
DSP_DR
MOM
LCL_CS_ADC*
ADC_CS*
DAC_Data_in
TP15
TP14
TP19
TP17
FS
LCL_CS_DAC*
LCL_CLKX
ADC_Data_n3
ADC_Data_out
DAC_Write*
ADC_TC*
ADC_Data_n3
ADC_Data_out
DSP_DX
ADC_TC*
START*
SAM*
DAC_Type
DSP_FSX
DSP_XF
RESET
SYSCLK
EVM_CLKX
INIT*
Q0
Q1
Q2
Q3
NC
R39
10K
START
SW2
U10
NE555D
OUT
RESET
DISCH
VCC
THRES
CONT
TRIG
GND
C60
0.1uF
C62
C61
R42
10K
R41
10K
RESET
SW3
TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243
TITLE:
Stand Alone
DOCUMENT CONTROL #:
6430333
REV:
Engineer: Joe Purvis
Drawn By: Joe Purvis
FILE: Stand Alone Mode
DATE: 28-Nov-2001
SIZE: A4
SHEET: 10 OF: 14


Revision History
REV
ECN Number
Approved
2
040500
Signal Conditioning
IN_0
OUT_0
Prototype Area
BB_Output_0
IN_0
W4
W3
W11
R9
33
TP7
Channel_0
C8
6800pF
BNC_0
W1
IDC_0
J3
1
B204+
B2_OUT
5
2
B203+
B2_FLT
6
3
B202-
4
B201-
8
B2/SD
W2
Signal Generator
Test signal 0
Test signal 1
W6
11
A2/SD
18
A201-
17
A202-
16
A203+
A2_OUT
13
BNC_1
W5
15
A204+
A2_FLT
14
+Vs
7
V2+
IDC_1
12
V2-
-Vs
9
VREF2
10
GND
W7
R12
33
TP6
Channel_1
C9
6800pF
Signal Conditioning
OUT_1
IN_1
Prototype Area
BB_Output_1
IN_1
W8
W25
TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243
TITLE:
Input Configuration
DOCUMENT CONTROL #:
6430333
REV:
Engineer: Joe Purvis
Drawn By: Joe Purvis
FILE: Input configuration
DATE: 28-Nov-2001
SIZE: A4
SHEET: 11 OF: 14


Revision History
REV
ECN Number
Approved
2
040500
+Vs
C6
10uF
C5
0.1uF
U3
V+
Duty adj.
Duty Adj.
Sine Out
Sine Adj
Sine Adj
Square Out
Timing Cap.
FM Sweep Input
FM Bias
Triangle Out
Not Connected
Not connected
V- / GND
ICL8038
R60
49.9K
R72
49.9K
W9
C17
1nF
C18
10uF
C15
0.1uF
-Vs
TP5
RV3
100K
R5
4.7K
R8
4.7K
U4A
TLE2082D
C13
0.1uF
C12
0.1uF
Test Signal 0
RV4
10K
C7
0.1uF
R59
4.7K
R7
4.7K
TP8
RV6
100K
R16
4.7K
R61
4.7K
U4B
TLE2082D
Test Signal 1
RV5
10K
C16
0.1uF
R13
4.7K
R15
4.7K
TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243
TITLE:
Signal Generator
DOCUMENT CONTROL #:
6430333
REV:
Engineer: Joe Purvis
Drawn By: Joe Purvis
FILE: Signal Generator
DATE: 28-Nov-2001
SIZE: A4
SHEET: 12 OF: 14

Revision History		
REV	ECN Number	Approved
2	040500	

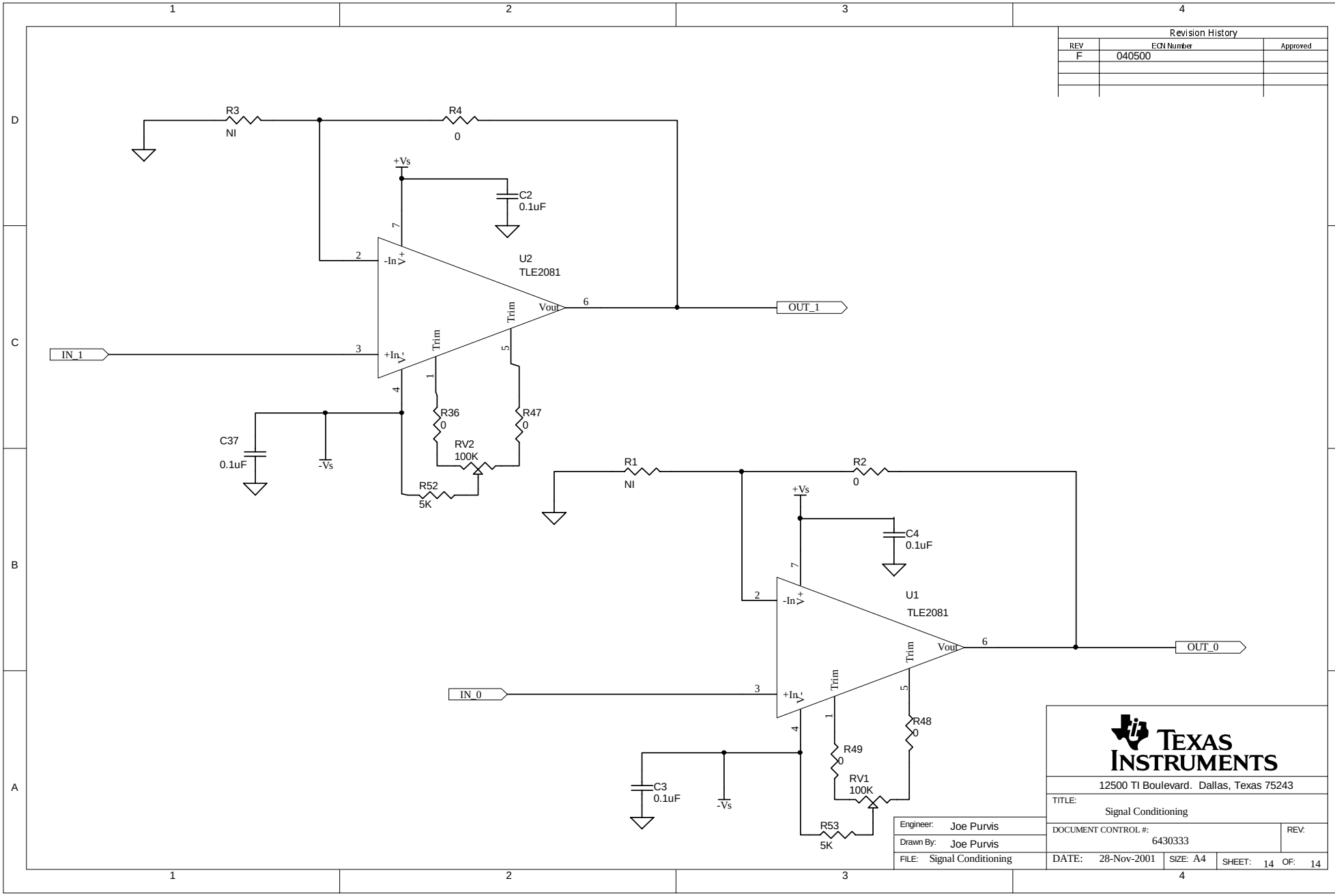




TEXAS INSTRUMENTS

12500 TI Boulevard. Dallas, Texas 75243

Engineer: Joe Purvis	TITLE: Prototype Area		
Drawn By: Joe Purvis	DOCUMENT CONTROL #: 6430333		REV:
FILE: Prototype Area	DATE: 28-Nov-2001	SIZE: A4	SHEET: 13 OF: 14


Revision History
REV
ECN Number
Approved
F
040500
R3
NI
R4
0
+Vs
C2
0.1uF
U2
TLE2081
-In
+In
Vout
Trim
OUT_1
IN_1
R36
0
R47
0
RV2
100K
R52
5K
C37
0.1uF
-Vs
R1
NI
R2
0
C4
0.1uF
U1
TLE2081
OUT_0
IN_0
R48
0
R49
0
RV1
100K
R53
5K
C3
0.1uF
TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243
TITLE:
Signal Conditioning
DOCUMENT CONTROL #:
6430333
REV:
Engineer: Joe Purvis
Drawn By: Joe Purvis
FILE: Signal Conditioning
DATE: 28-Nov-2001
SIZE: A4
SHEET: 14 OF: 14